Solid Freeform Fabrication 2016: Proceedings of the 27th Annual International Solid Freeform Fabrication Symposium – An Additive Manufacturing Conference
Reviewed Paper

ADDITIVE MANUFACTURING OF HIGH RESOLUTION EMBEDDED ELECTRONIC SYSTEMS

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Abstract

Additive Manufacturing (AM) processes can facilitate the rapid iterative product development of electronic devices by optimising their design and functionality. This has been achieved by combining two additive manufacturing processes with conventional surface mount assembly to generate high resolution embedded multilayer electronic circuits contained within a 3D printed polymer part. Bottom-up DLP Stereolithography and material dispensing of isotropic conductive adhesives have been interleaved to deposit microscale features on photopolymer substrates. The material dispensing process has demonstrated the high density deposition of conductors attaining track widths of 134µm and produced interconnects suitable for directly attaching bare silicon die straight to the substrate. Interconnects down to a diameter of 149µm at a pitch of 457µm have been realized. In addition, this research developed a novel method for producing high aspect ratio z-axis connections. These were simultaneously printed with the circuit and component interconnects by depositing through-layer pillars with a maximum aspect ratio of 3.81. Finally, a method to accurately embed the packaged circuit layer within the printed part has been employed using bottom-up stereolithography.

Keywords: *additive manufacturing; process integration; multilayer embedded electronics; DLP stereolithography; material dispensing; flip chip packaging*

Introduction

Additive manufacturing technologies have been proven to provide substantial advantages over traditional manufacturing methods including greater process versatility, achievable geometric complexity and digitally driven fabrication capability. The application of these

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processes in electronics production helps to overcome the template driven nature of conventional electronics manufacturing processes that result in a lack of customisation and long pre-production timescales. Individual AM processes and materials are typically limited in their processing capabilities. Electronic devices that require the multi-material compatibility and components can therefore be printed by interleaving two separate processes capable of depositing both dielectric and conductive materials. Such a process capability would therefore provide a larger range of applications for embedded sensor systems, microfluidics and bespoke electronic devices.

Successful attempts to hybridise AM processes have been previously been conducted for the fabrication of electronics including the production of substrates by Stereolithography (SL), Ultrasonic Consolidation (UC) [1], Fused Deposition Modelling (FDM) [2], material jetting [3] and Selective Laser Sintering (SLS) [4] and; the deposition of conductors by aerosol jetting, ink jetting and dispensing based direct writing techniques [5].

The feasibility of embedding functional components using shape deposition manufacturing for build 3D end-use products was first explored in 1992 [6] and further adopted by Kataria and Rosen [7] who proposed a technique for embedding functional inserts in SL parts. The University of Texas at El Paso introduced a hybrid AM setup combining material dispensing of low viscosity conductive inks with laser-based top-down stereolithography [8][9][10]. Photopolymer substrates were produced with surface channels and trenches into which conductive ink could be deposited and laser cured and, components positioned and individually embedded. In addition, through holes were created during the SL process which were subsequently pumped with conductive ink [11]. These cavities inhibit the placement of small surface mount devices and therefore this technique does not lend itself to the production of high density multilayer electronics. FDM was then applied to this hybrid concept to build a 2.5D circuit board [12]. Niese *et al.* [13] presented a concept for encapsulation of PCBs and fabrication of metallic channels to route a power source using an Additive 3D Molded Interconnect Device (ADDMID) process, with Stereolithography using a doped photopolymer replacing injection moulding to create polymer parts for laser processing.

In 2016, Voxel8 released a material extrusion system with multi-material capability coupling Fused Filament Fabrication (FFF) and dispensing within a single printer [14]. This allows a polymer substrate and conductive material to be sequentially deposited creating a polymer package with internal electronics. Stratasys and Optomec also demonstrated direct writing onto conformal FDM substrates by aerosol jetting, printing circuits, sensors and antennas onto an unmanned aerial vehicle (UAV) [15]. FFF and FDM do however demonstrate disadvantages such as low resolution, weak adhesive strength between layers, poor surface finish due to stair stepping and difficulty producing hermetic structures [16].

Finally, non-polymer based technologies have been investigated for use in hybrid additive manufacturing of electronics. Ultrasonic consolidation has been used to embed

electronics within three dimensional metal structures [17][18][19] and, ink jetting has been used to print conductive inks into additively manufactured ceramic substrates [20].

This paper introduces a new digitally driven method developed for the fabrication of functional multilayer electronics devices. Conductors can be printed directly onto the surface of a photopolymer substrate, with no need for features to control the deposition of material or position of components. Dispensed circuitry and low temperature assembled and packaged electronic components can be embedded within a thick layer of photopolymer. During this work investigations have been conducted to:

- characterise the dispensing process for the production of conductive traces, pillars and interconnects
- optimisation of the electrical properties of the printed conductors
- analysis of the interaction between conductive materials and photopolymers
- proving the application of this manufacturing technique for flip chip packaging

Finally demonstrators in the form of multilayer flashing 555 timer circuits are presented to prove the technological capability.

Hybrid Additive Manufacturing Process

Figure 1(a)-(h) shows the hybrid manufacturing process flow beginning with the fabrication of acrylic-based photopolymer substrates using bottom-up DLP stereolithography. A mid-process developing technique including ultrasonic agitation is then utilised to decontaminate and optimise the substrate surface quality for dispensing. This process is compatible with surface mount assembly, a consequence of the utilization of isotropic conductive adhesives (ICAs) to form conductive traces, novel freestanding through-layer pillars and component interconnects allowing surface mount devices (SMDs) to be deposited directly onto the bond pads. After surface mount assembly, the ICA is thermally cured, encapsulated within a thick layer of photopolymer and a new cavity fabricated to locate the next layer of circuitry.

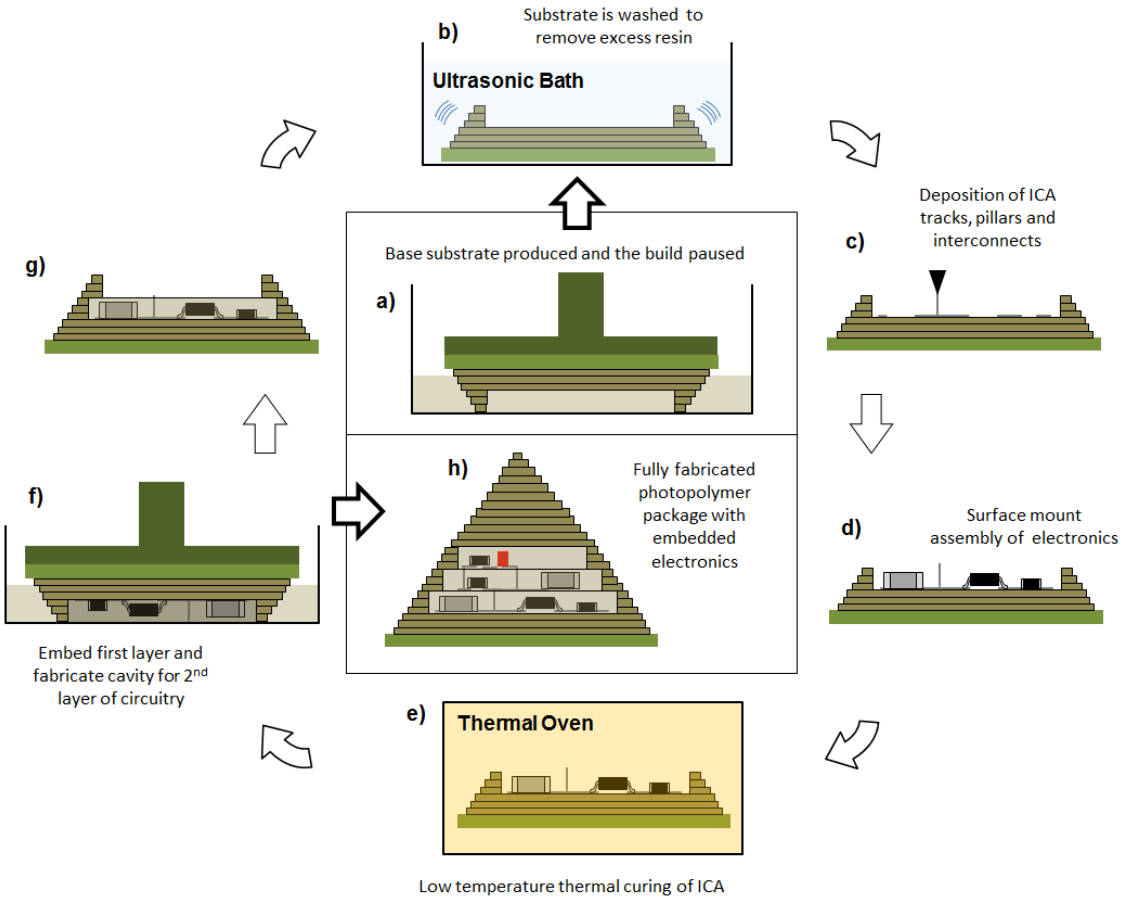

Figure 1. Hybrid AM Process Chain

Multilayer Photopolymer Substrate Fabrication

The Stereolithography system utilises a DLP pico-projection mechanism with a Digital Micromirror Device (DMD) [21] dynamic mask and an ultraviolet (UV) 405nm LED source. This light source is arranged in a bottom-up orientation, with the projector focused on the base of the material vat and an average light intensity of 0.962mW/cm^2, requiring a 10 second exposure to cure a 100µm thick layer of photopolymer. DLP control software also facilitates an increase in the light intensity to 3.16mW/cm^2 however; this consequently causes faster deterioration of the anti-stiction PDMS layer on the vat base and has been proven to degrade the reflective coating of the DMD. The setup provides a resolution of 109µm over a 140mm x 87mm projection area and, customisable z-axis layer thickness. This approach results in a faster build time than vector scanning methods and, when combined with the bottom-up projection orientation results in a substrate surface roughness (R_a) of 2µm and an average change in surface height of 6µm over a 15mm x 15mm sample area. This high quality is achieved due to its proximity to the PDMS layer on the base of the vat during curing. The photopolymer is an acrylic-based broad-band resin sensitive to wavelengths of light up to 440nm and has a glass transition temperature of ~100°C.

Mid-Process Substrate Developing

To facilitate the integration of Stereolithography with additional AM processes, decontamination of the substrate surface is required to ensure the successful deposition of conductive materials onto the photopolymer. Ultrasonic agitation in a solvent was identified as the most efficient method of thinning and removing excess liquid resin from the substrate surface. Specimens fabricated using the broad-band acrylic-based photopolymer exhibited surface cracking after exposure to a number of common solvents compromising their surface quality due to incomplete polymer crosslinking. Alternative solvents and additional photoresist processing steps including relaxation and thermal baking in addition to an UV oven exposure were investigated for their effect on the substrate surface quality [22].

Photopolymer samples were exposed for 5 minute, 30 minute, 2 hour and 24 hour time periods to eight different solvents:

1. Isopropyl Alcohol (IPA)
2. Methanol
3. Acetone
4. D-Limonene
5. Xylene
6. Ethanol
7. Toluene
8. Tetrahydrofuran

D-Limonene and IPA showed no degradation of the sample or its features however, surface cracking was demonstrated on every specimen. Relaxation and thermal baking resulted in a small reduction in the frequency of cracking however, 30 minutes flood exposure to light in a UV oven after solvent rinsing in D-Limonene resulted in elimination of the cracking as shown in Figure 2.

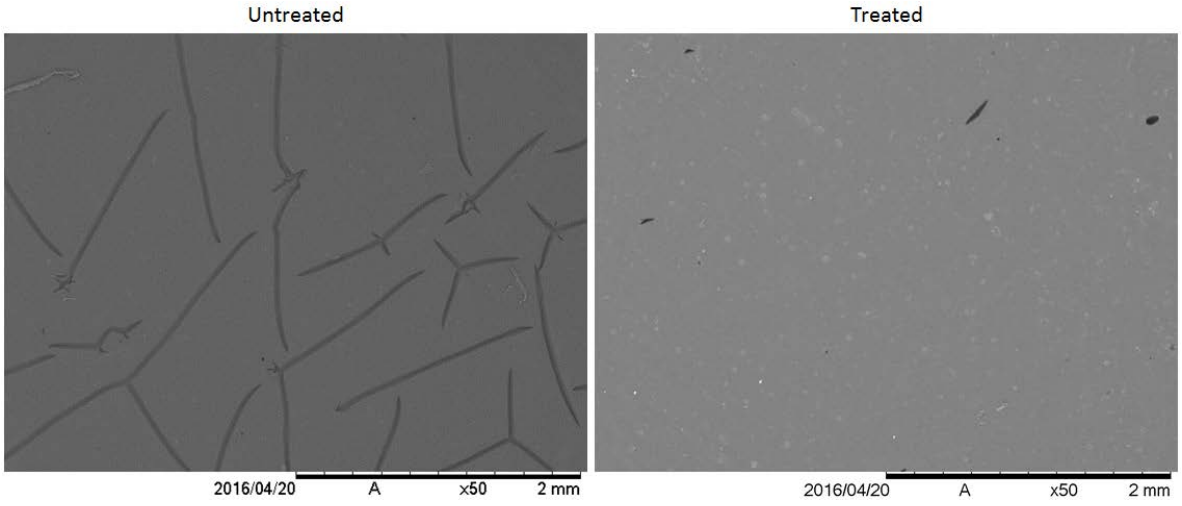

Figure 2. Comparison between unprocessed and processed substrate surfaces

This is a result of the continuation of crosslinking and therefore prevention of solvent penetration in the substrate. Optimal surface quality was therefore achieved by 2 minutes of ultrasonic agitation in D-Limonene and 30 minutes flood exposure in a UV oven.

Dispensing Conductors

A Musashi Shotmaster 500 dispensing system with a Musashi Super$\Sigma^{®}$CMII digital pressure controller was used to print conductors on photopolymer substrates. The system is comprised of five main parts:

- a 3-axis CNC router
- a computer controller
- a digitally controlled dispenser
- an alignment camera
- a laser positioning feedback system

When combined, these parts are capable of depositing high viscosity, heavily loaded ICAs with viscosity up to 1,000Pa.s with printing pressures between 30kPa to 500kPa and speeds of 0.1mm/s to 300mm/s at a movement resolution of ±5µm. Printing is controlled in 3 axes and a laser is used to map the surface of the substrate, automatically adjusting the nozzle height to maintain a constant print gap.

Two commercially available silver based isotropic conductive adhesives, Epotek E4110-PFC and Epotek EJ2189 with maximum particle sizes of ≤20µm and ≤45µm [23][24], were selected due to their rheological properties and low temperature curing requirements, making them compatible with SL photopolymer materials. Control over the deposition of these ICAs can be achieved through a combination of five parameters: 1) viscosity of the dispensed material; 2) inner diameter (ID) of the dispensing nozzle; 3) extrusion pressure; 4) print speed and; 5) print gap (distance between the nozzle tip and substrate).

Conductors have been identified for fabrication using the combination of material dispensing and ICAs. Conductive traces were printed to connect multiple discreet components and integrated circuits (ICs) and, bond pads deposited on which these components can be placed. In addition, to facilitate the production of multilayer embedded electronics, a new method for the production of through layer connections has been developed. Freestanding pillar structures were printed in the z-axis in sequentially deposited layers, to produce features capable of spanning the maximum 2mm distance between two adjacent layers of circuitry.

Electronic Packaging

Surface mount assembly (SMA) is highly advantageous as it is the most commonly used packaging method due to its low cost, high throughput and high density capability. This technique allows components to be attached directly onto surface of printed circuit boards, functionality that is also demonstrated by this hybrid process as components can be mounted

onto dispensed ICA interconnects on the photopolymer surface. The achievable printing resolution of the dispensing process determines the SMD size that can be mounted onto the deposited bond pads, with this process demonstrating the packaging of both 1206 and 0603 SMDs. In addition, ICs with pins at pitches of 1.27mm and 500µm have been mounted. The height of these components determines the necessary embedding layer thickness identified as 2mm and 1.2mm for larger and smaller devices respectively and therefore, the height of the conductive pillars.

The electronics industry is driven by demand for the minimisation of circuitry and therefore, this hybrid AM process chain has been adapted, as shown in Figure 2, for use in flip chip packaging. This packaging technique is an evolution of SMA where bare microchips, predominantly semiconductors, are attached face down onto a substrate reducing weight, making the device thinner and achieving a higher input/output density due to smaller pitch between an array of bond pads [25]. This functionality has been proven using daisy chain patterned bare die, requiring alternate bond pads to be contacted to create a complete electrical connection around its perimeter. Substrates were fabricated with 600µm x 200µm x 200µm (Length x Width x Depth) channels in the surface corresponding to the daisy chain pattern, ultrasonically agitated in solvent and filled with an ICA before low temperature thermal curing. The surface was then lapped to planarise and remove any excess conductive materials from the substrate surface. ICA interconnect bumps were then deposited on either end of each filled channel before the bond pads on the bare die were aligned with the bumps, the bare die placed and a bonding force applied to the chip.

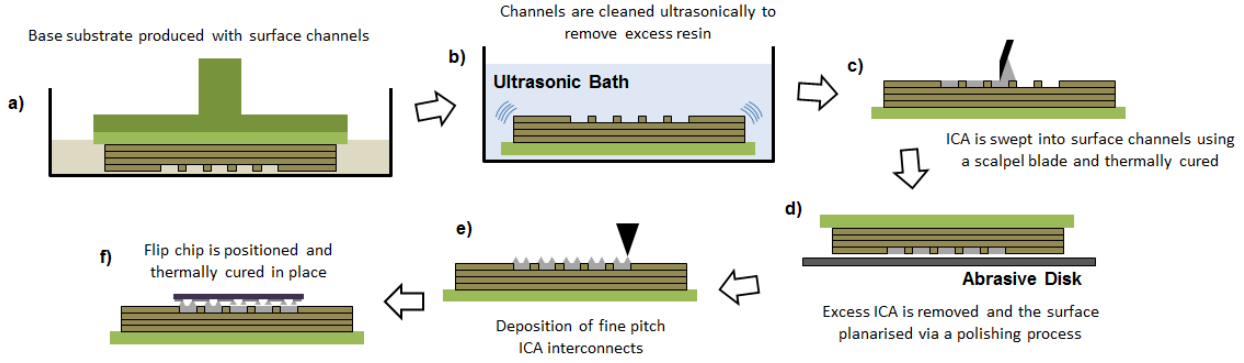

Figure 3. Flip chip packaging via hybrid AM

The substrate fabrication technique allows embedding of the electronics in a thick layer of photopolymer. This provides a high quality surface with exposed through layer connections for the dispensing of subsequent layers of circuitry. One benefit of the Stereolithography process is its ability to produce geometrically complex structures, an advantage that can be maintained after hybridisation by fabricating external sidewalls surrounding a cavity in which circuitry can be deposited as shown in Figure 3. These cavities can then be submerged in liquid photopolymer facing upwards causing de-gassing and SMD underfilling. The substrate is inverted and immersed in the material vat, pressing the tips of the conductive pillars into the PDMS layer on

its base. Finally, the filled cavity is selectively exposed to UV light for a prolonged period of time after which a subsequent cavity is fabricated for the next layer of circuitry.

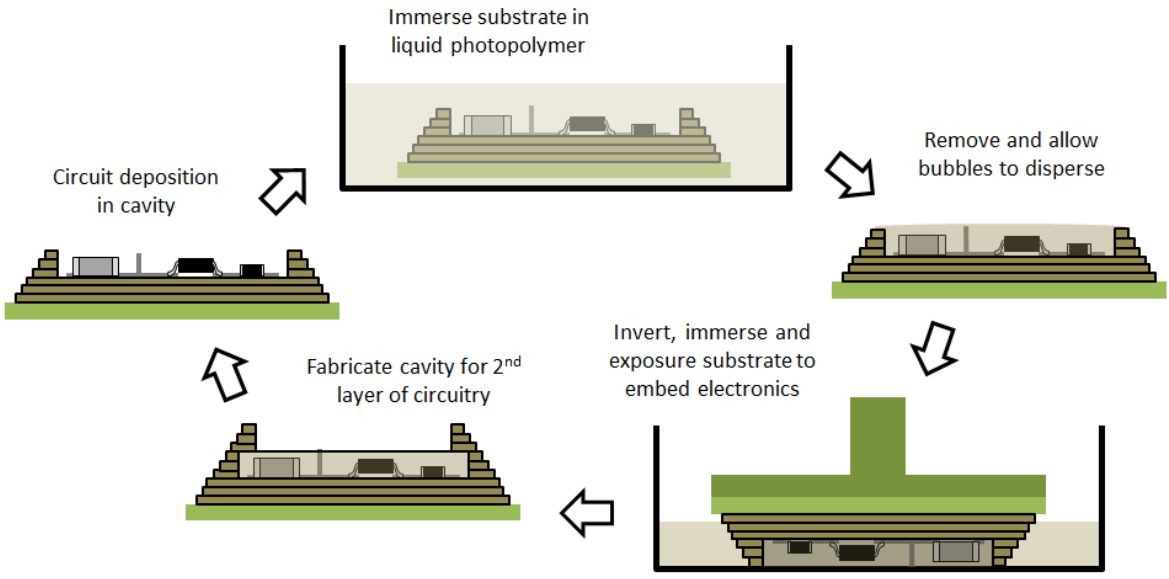

Figure 4. Process of embedding electronics using Stereolithography

Characteristics of Dispensed Conductors

Printing parameters can cause significant differences in the size and quality of the conductors and have been characterised in their production of conductive traces, z-axis through layer pillars and flip chip interconnects. The objective was to print repeatable features of the smallest possible size enabling the size of the packaging and circuit footprint to be minimised.

Conductive Traces

Regardless of the resistivity of the conductive adhesive, line resistance can be controlled through the track geometry, with increased cross sectional area reducing the line resistance. Tracks were printed on the substrate surface in both ICA materials to determine the effect of printing pressure, print speed and nozzle size on their behaviour and appearance. A 10x objective lens was used to obtain profile data of sets of five conductive traces printed in different combinations of parameters. The width and peak height of these tracks were then extracted from this data. Higher viscosity E4110-PFC conductive adhesive produced a smoother surface finish and more semi-circular profile. Data presented in Table 1 shows that in higher volume deposits E4110-PFC showed a higher aspect ratio than lower viscosity EJ2189 due to material slumping however, as the nozzle inner diameter is decreased and the dispensed volume reduces, this slumping effect is reduced resulting in higher aspect ratios printed in EJ2189.

Table 1. Comparison of aspect ratios produced by E4110-PFC and EJ2189 ICAs

Nozzle Size (µm)	E4110-PFC		EJ2189	
	Avg. Width (µm)	Aspect Ratio	Avg. Width (µm)	Aspect Ratio
100	234	0.278	218	0.300
200	370	0.315	363	0.306
250	419	0.387	420	0.356

The smallest tracks produced were 134µm in width and 38µm in height. These were printed in the lower viscosity EJ2189 ICA at a pressure of 140kPa, 7mm/s print speed and 100µm nozzle ID. The lowest trace dimensions in E4110-PFC through a 100µm nozzle ID were 170µm width and 42µm height printed at 300kPa and 7mm/s print speed. These track widths enable fine pitch conductors to be printed reducing the size of compatible electronic components and the corresponding package.

The lowest resistivity possible is desired to reduce the line resistance of conductors while minimising their size. Conductive adhesives achieve their conductivity through two mechanisms, shrinkage of the resin part of the epoxy formulation increasing contact between particles or flakes of the conductive filler materials and, evaporation of lubricants further reducing the distance between conductive particles [26]. Three different low temperature thermal curing regimes listed in Table 2 had their effect on material resistivity measured. The glass transition temperature of the photopolymer limited the processing temperature to 100°C.

Table 2. Manufacturer's specified and chosen experimental curing regimes for ICA materials

	E4110-PFC Spec		EJ2189 Spec		Experimental Regimes	
	Temp (°C)	Time (hrs)	Temp (°C)	Time (hrs)	Temp. (°C)	Time (hrs)
Low	45	6	23	72	45	6
Med	80	3	80	3	80	3
High	120	1	100	1	100	1

Optical microscopy was used to capture the topology of track samples produce in both ICAs and cured using all three regimes. The resulting clouds of data points were processed using a custom MATLAB® code designed to compute the average cross sectional area of each measured length of track. Track resistance (R), track length (L) and cross sectional area (A) were then substituted into equation 1 to calculate the resistivity (ρ):

$$R = \rho \frac{L}{A} \quad (1)$$

In both materials, higher temperature processing at 100°C for 1 hour resulted in lower resistivity with EJ2189 demonstrating a resistivity of ~2.8×10^{-4} Ω.cm compared to ~4×10^{-4} Ω.cm in E4110-PFC. This difference between the two ICAs is shown across all curing regimes in

Figure 4. One explanation for this lower resistivity in EJ2189 is its use of flakes as opposed to particles, creating a greater contact area between adjacent flakes.

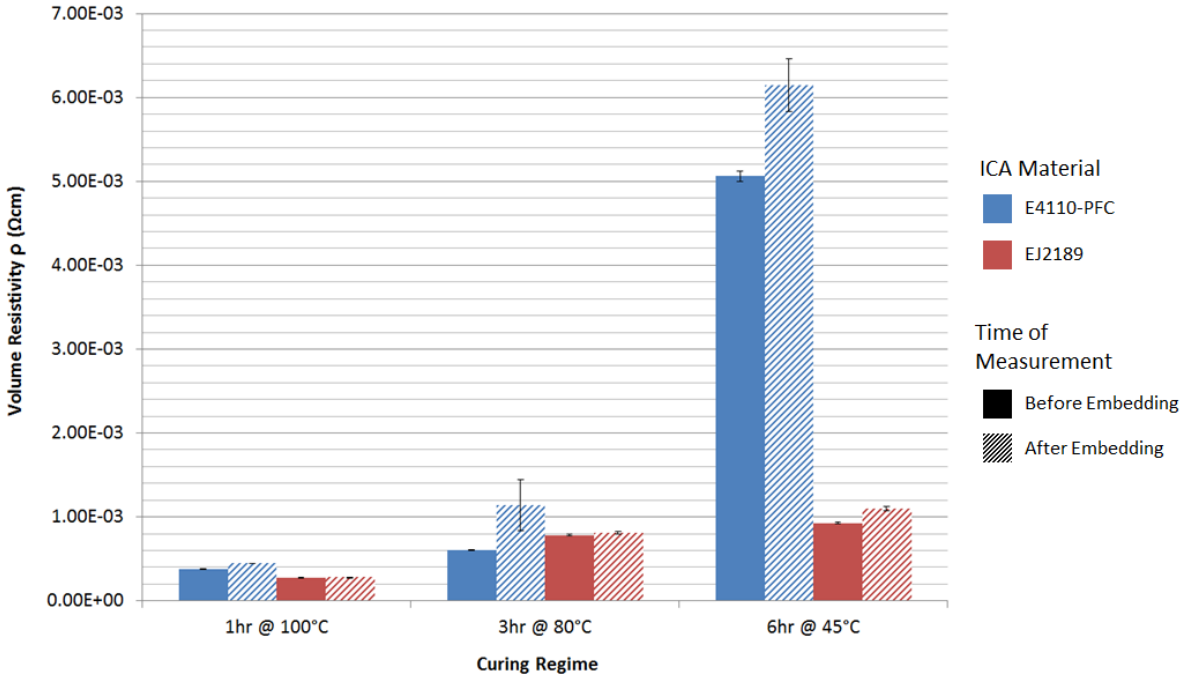

Figure 5. Effect of different curing regimes and embedding on ICA volume resistivity

After embedding in a thick layer of photopolymer, both ICAs exhibited an increase in resistivity however, the average increase across all regimes in EJ2189 was just 8% compared to 23% in E4110-PFC. After curing at the highest temperature some degradation of the SL substrate was evident and therefore, 80°C for 3 hours was adopted as the default curing regime.

Conductive Pillars

Vertical conductive structures were introduced to realise conductive connections between the multiple layers of stacked circuitry. The printing of these structures was facilitated by the viscosity of the ICA materials and the three axis capability of the dispensing equipment. Figure 5 shows the clockwise square helix design of the conductive pillar and proportional alterations made to the pillar dimensions when printed through the three available nozzle IDs.

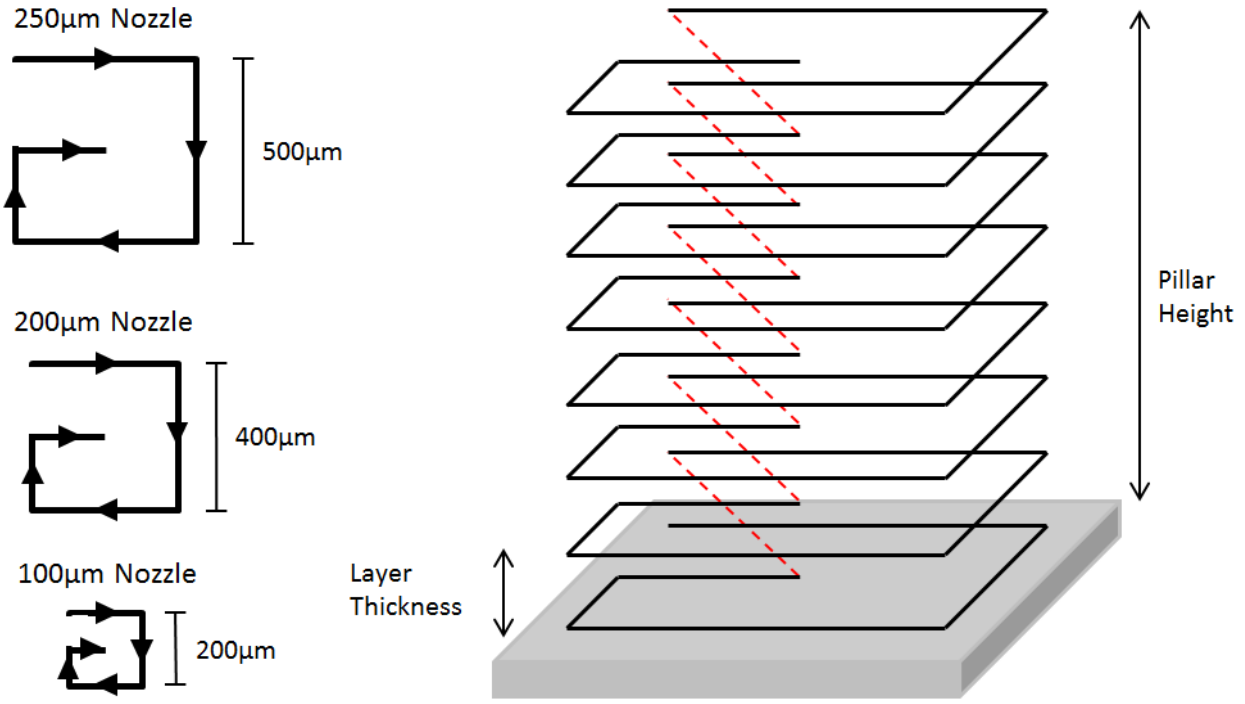

Figure 6. Conductive pillar design and dimensions

Material slumping demonstrated during track deposition was also exhibited during pillar printing and, due to the multiple layers of successive dispensing and additional weight of these layers, the effect was exaggerated. Higher viscosity E4110-PFC slumped less and therefore produced higher aspect ratio, taller and narrower structures. Printing characterisation was conducted using printing pressure, print speed and nozzle ID as variables to determine the optimal combination of parameters for each square helix design shown in Figure 5. Once the printing behaviour and materials had been assessed, additional layers could be added to each design one by one, increasing the height until the printed structure collapsed at its height limit.

Figure 6 showed that E4110-PFC created the tallest structures using each of the three nozzle sizes. 16, 18 and 24 layers were printed through 250µm, 200µm and 100µm nozzle IDs resulting in aspect ratios of 3.81, 3.23 and 3.68. The 100µm nozzle ID produced a pillar in excess of 2mm in height and 553µm wide, making it suitable to span the thickest proposed 2mm embedding layer in this investigation while minimising the footprint on the substrate. The maximum aspect ratio achieved using lower viscosity EJ2189 was 2.41 with a height of 1.175mm over 17 layers.

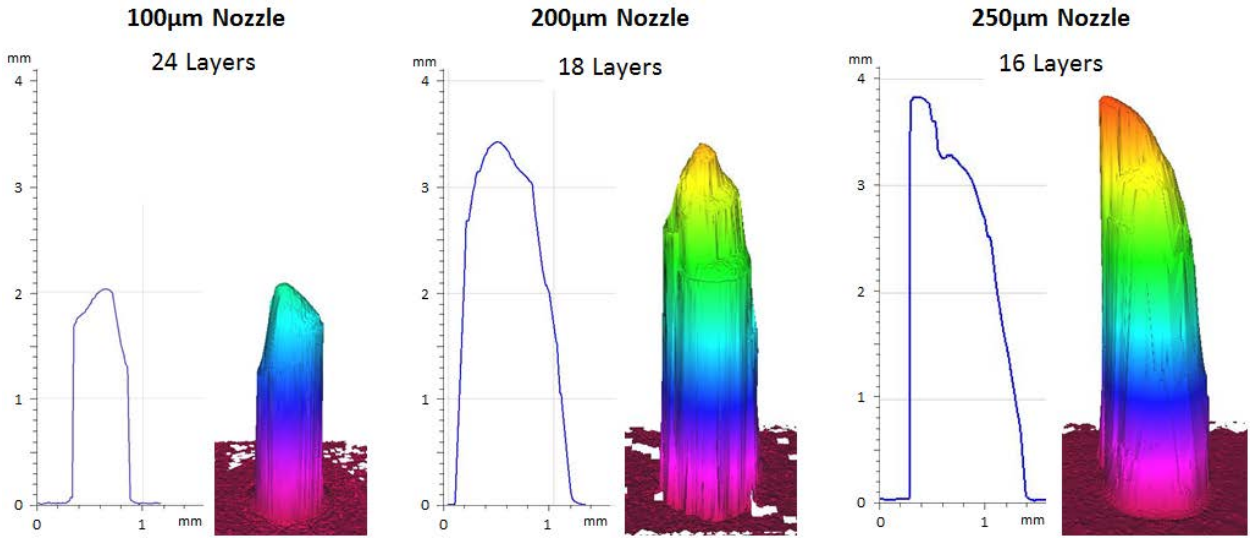

Figure 7. Topologies of maximum pillar heights produced using each nozzle ID

Flip Chip Interconnects

The deposition of flip chip interconnects onto a substrate surface is conducted by timed point deposits, differing from trace and pillar dispensing as there is no nozzle movement during the application of pressure to the ICA. For the purposes of this process characterisation, print gap and pressure actuation time were introduced as variables and, print speed removed. The lower viscosity of EJ2189 demonstrated better wetting behaviour than E4110-PFC as it separated from the nozzle more easily, allowing smaller volumes of ICA to be deposited and therefore smaller bumps to be produced. Figure 5 shows the smallest consistent interconnects produced with an average width of 149µm and height of 80µm. They were printed with a combination of 0.2s pressure actuation time, 30kPa pressure and 60µm print gap in EJ2189.

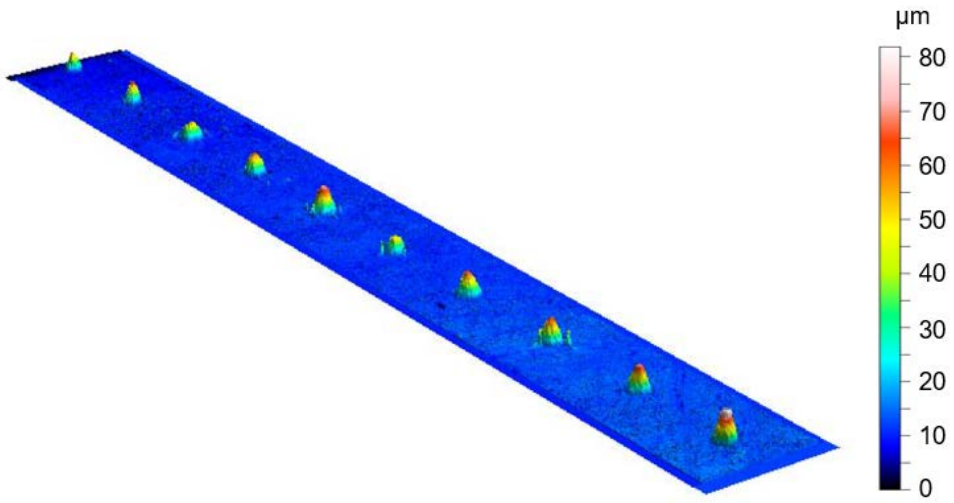

Figure 8. Smallest flip chip interconnects with consistent profile

The adaptation of this hybrid AM process for flip chip packaging was validated using daisy chain connections and a bare silicon test die. This set-up provides a mechanism by which contact resistance between adjacent connections can be measured. The sourced bare die were only available pre-bumped with solder, features made unnecessary by the ICA interconnects however, the success of this flip chip packaging process could still be proven. Figure 8a shows redistribution traces designed into the substrate surface allowing the resistance of each individual connection to be measured. The resistance of each connection reduced from 5.2Ω to 2.3Ω by adding a 0.08N bonding force and removing the solder bumps that increased the length of the conductive pathway. The solder removal also reduced the chip standoff from 160µm (Figure 8b) to 80µm, indicating the distance between the surface of the substrate and underside of the bare die.

In traditional electronics assembly, an insulating polymer is used to fill the void between a chip and the substrate protecting interconnects from stresses such as vibration or shock [27]. The embedding process introduced as part of this hybrid AM technique has also been used to underfill flip chip packaged bare die with photopolymers, with no measurable change in contact resistance. Figure 8c and Figure 8d shows cross sectional micrographs of successfully underfilled bare die at a standoff height of 160µm. The same process conducted on die with an 80µm standoff showed bubbles trapped between the substrate and chip. Ultrasonic agitation is one technique that could be investigated further for used in removing this trapped air.

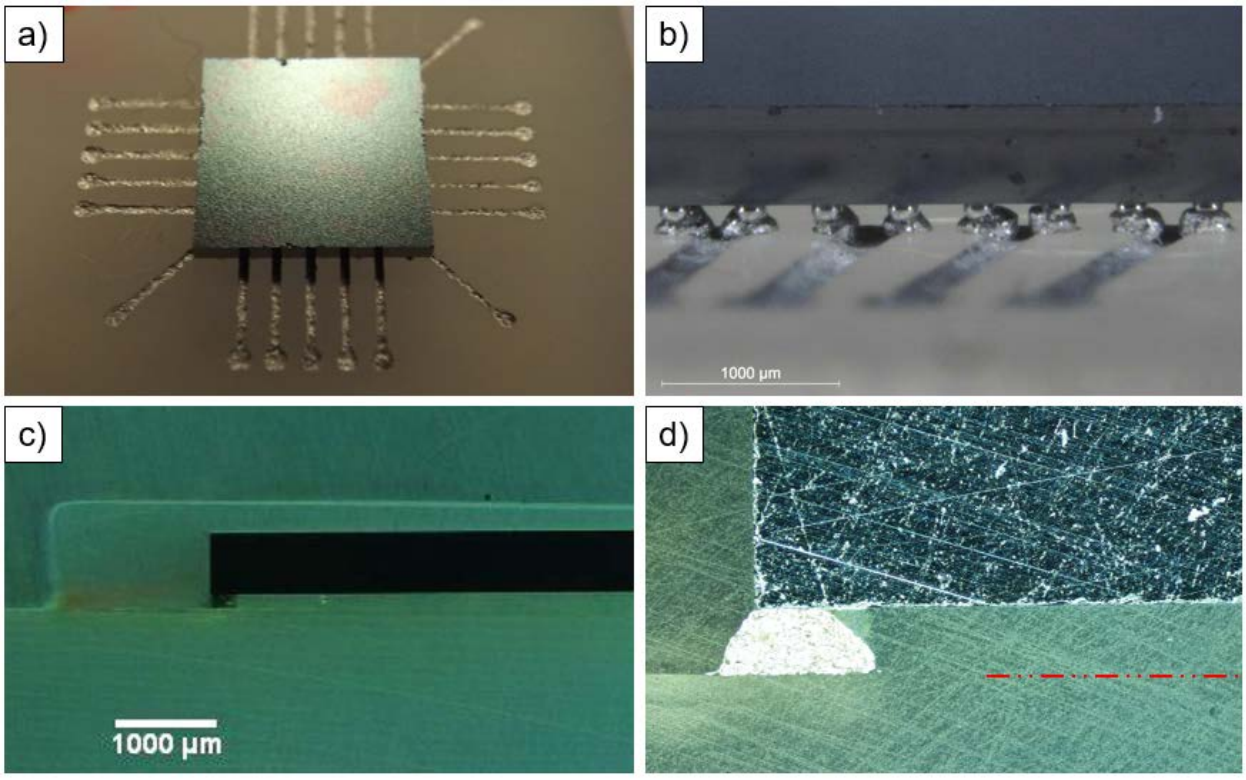

Figure 9. Flip chip packaging and underfilling of daisy chain bare die

Demonstrators

Processes and methods for interleaving multiple additive manufacturing techniques have been developed. These processes have been designed to produce conductive tracks, interconnects and z-axis connections. A flashing 555 timer circuit was selected to demonstrate the application and integration of these processes. It provides a simple and visual exhibition of this hybrid manufacturing capability and, embedding of a variety of surface mount devices including discrete components (resistors and capacitors), an actuator (LED) and a small outline integrated circuit (555 timer chip).

Feasibility Demonstrators

Initial demonstrators were designed to evaluate the effectiveness of the integration of multiple processes and therefore no not demonstrate the geometric capabilities of this manufacturing technique. Figure 9 shows single, double and triple layer feasibility demonstrators, all of which flashed as designed when a power source was applied, proving that ICA conductors and SMDs could be successfully embedded on multiple layers within a photopolymer substrate. In addition, the triple layer device was the first to utilise a miniaturised circuit layout decreasing the footprint of printed conductors from 25mm x 15mm to 9mm x 9mm and halving the size of SMDs from 1206 to 0603 (imperial code, resistor dimension of 1.6mm x 0.8mm x 0.8mm) and, reducing the size of IC pin pitch from 1.27mm on a Mini Small Outline Package (MSOP) to 500µm on a Thin Shrink Small Outline Package (TSSOP).

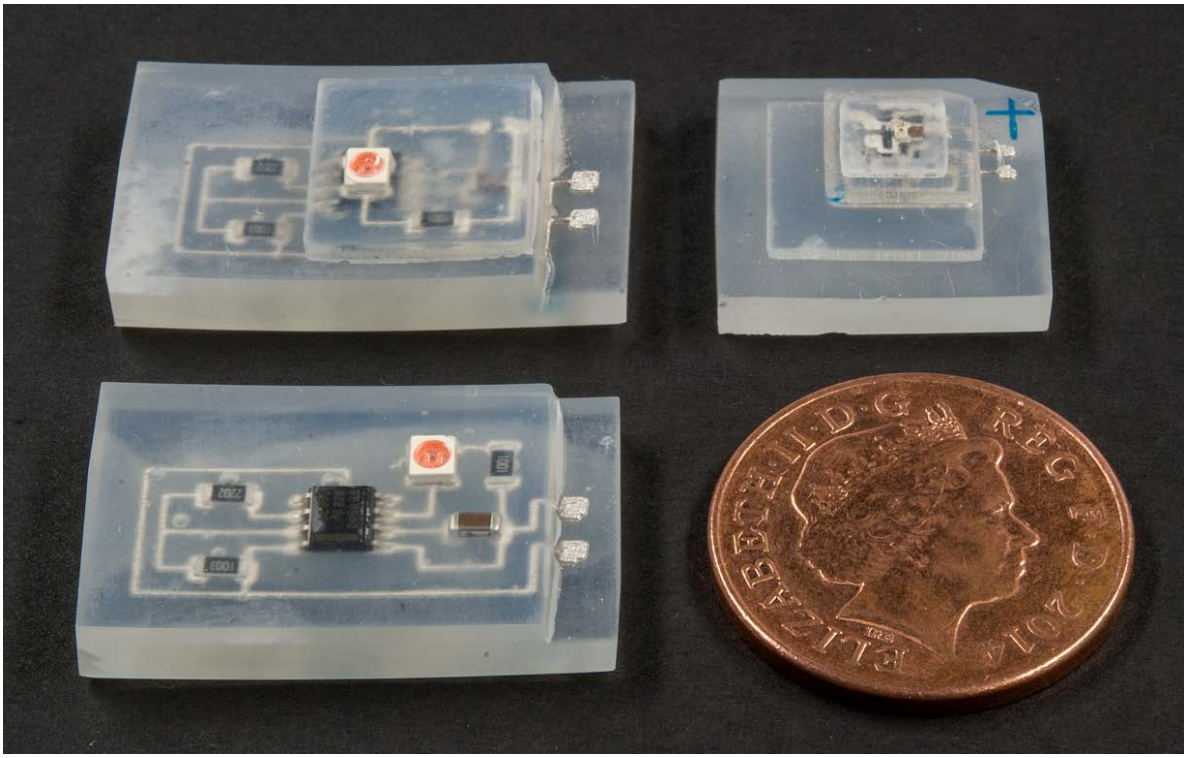

Figure 10. Single, double and triple layer feasibility demonstrators

Pyramid Demonstrators

Following the demonstration of successful fabrication and function of the integrated AM processes, the capability of this technique to produce high complexity packaging geometries with internal electronics was explored. A pyramid shape was chosen as it displays a constant change in external geometry that could only be achieved using this technique. Initially, a 30mm x 30mm pyramid base was designed (Figure 10a) and built (Figure 10b) with a cavity in which circuitry could be deposited before embedding and, the subsequent production of the next cavity enclosed within external side walls. The characterisation of conductor deposition allowed a reduction in size of the pyramid base (Figure 10c) to 15mm x 15mm with ICAs deposited using a 100µm ID nozzle. Finally, this process cycle was repeated to completion of the circuit at which point the peak was fabricated to fully encapsulate the electronics and complete the fully functioning pyramid demonstrators (Figure 10d) that flash intermittently when connected to a power source.

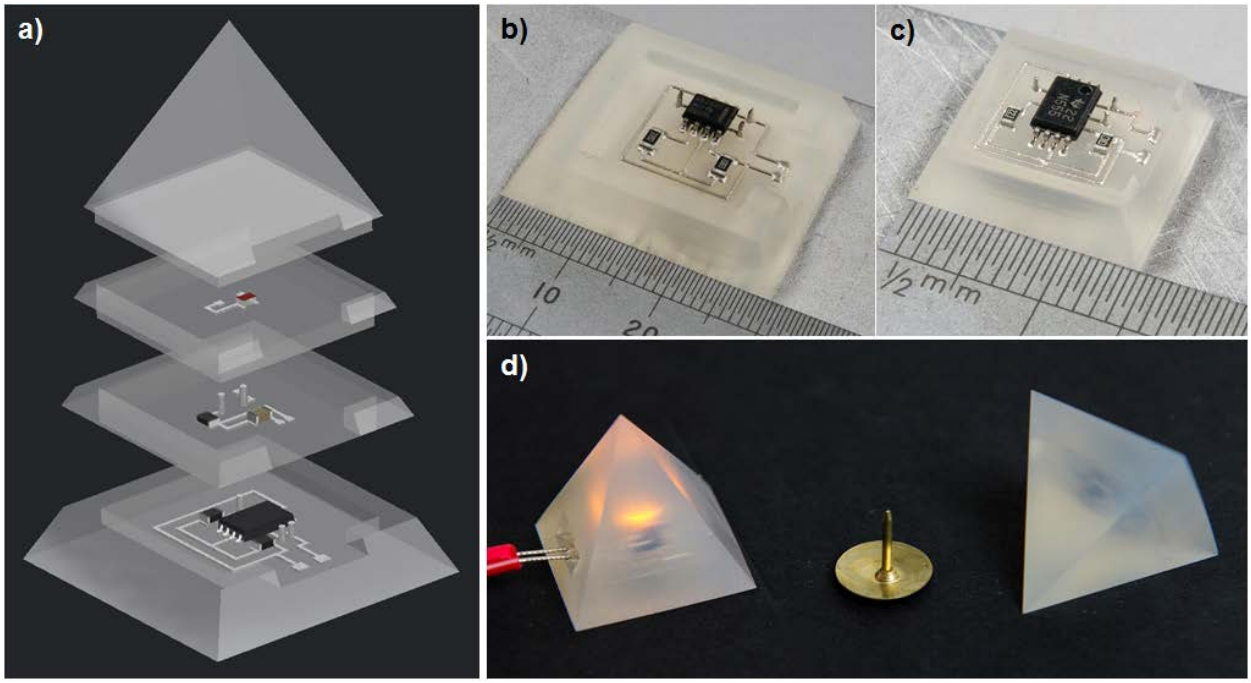

Figure 11. Pyramid a) CAD design, b) 30mm x 30mm base, c) 15mm x 15mm base and d) fully functional demonstrator

Conclusions

A novel hybrid manufacturing process has been presented showing the integration of Stereolithography and direct writing technologies with a mid-process developing procedure and conventional SMA of discrete electronic components, actuators and integrated circuits.

A DLP Stereolithography system in a bottom-up orientation was applied to the fabrication of electronic substrates and the packaging of electronics within thick layers of cured photopolymer. Curing the resin in contact with the base of the vat results in high quality surface finishes on both the initial base substrate and subsequent thick embedding layers.

High viscosity, low temperature curing isotropic conductive adhesives were combined with material dispensing to produce conductors including tracks, interconnects and, novel freestanding conductive pillars designed to create through layer conductive connections. Surface mount devices could be mounted directly onto the printed bond pads before they were thermally cured at 80°C for 3 hours, resulting in a higher conductivity than specified by the manufacturer. When embedded within the polymer matrix, SMDs were underfilled, tips of conductive pillars pushed into the soft PDMS layer on the vat base and, only an 8% increase in ICA resistivity was observed. In addition to surface mount packaging, chip scale flip chip packaging has been conducted using a combination of Stereolithography and dispensing techniques to produce 600µm x 200µm x 200µm conductive trenches with 149µm flip chip interconnects. Bare die have also been successfully underfilled using the liquid photopolymer to reduce stresses on the ICA interconnects.

This hybrid additive manufacturing process has been successfully used to fabricate geometrically complex pyramid demonstrators with internal triple layer flashing 555 timer circuits and, package flip chip bare die. This technology could therefore be used to realise bespoke electronics in complex packaging for application in such scenarios as embedded sensor systems, mechatronics and lab on chip or microfluidics.

Acknowledgements

This work is funded by the UK Engineering and Physical Sciences Research Council under grants EP/L017431/1, EP/L017350/1, EP/L016907/1 and EP/L017415/1.

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